

Appendix H1

MORE REALITY TALES ABOUT PCB FABRICATION

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Consider the following if you think you understand prototype PC boards. The following E-mail is from the Ken Willis via the Signal Integrity email-reflector list.

Subject: RE: [SI-LIST]: Possible TDR microstrip measurement error?

Hi Eric,

I was just starting to write some of the same comments when I read this message from John. I started out in PC fab way back when, and built and TDR'd more impedance controlled boards than I want to remember (still recovering from the fumes coming off the cupric chloride etch line). Meeting microstrip impedance specs was usually a bit more challenging, for a couple of reasons.

We were doing mostly foil construction externally, so that first dielectric was usually prepreg instead of pre-cured core material, so you'd get some variation there in thickness.

Boards electroplate from the "outside in", so you get variation in trace thickness across the panel. The impedance coupons are always on the edge of the board, so they plate up pretty high. If you start with 1/2 oz copper (.7 mils), it would generally plate up to 2.1 or so.

If you get variation in trace height, you will also get variation in finished trace width due to the etching process. Taller traces will see less line width reduction but more trapezoidal shape than the lower ones.

Most of our boards then were SMOBC (solder mask over bare copper), so in theory you should be designing them as buried microstrips, with a couple mils of soldermask over the traces, then air. But try getting ϵ_r values from a soldermask vendor. I didn't have any luck, so empirically you TDR the boards after external etching, and make sure you are 3 ohms or so over nominal. Then applying the mask generally dropped the measurement back into mid-range.

So you add all these variables up, plus the mistake some may make of using ϵ_r of FR4 above and below the trace in the model, and you have a recipe for confusion. Hence the empirically derived fudge factors by every fab shop.

My recommendation to those on the SI list is that if you really have traces where the Z_0 is that critical, do NOT put them on external layers. There is too much process variation there. You will get a lot more consistency on non-plated 1/2 oz. inner layers. And don't kid yourself into thinking that because you spec'd external layers $\pm 10\%$ that you got it. You have probably just bought a batch of impedance-controlled coupons. There will be significantly more variation in thickness, line width, and Z_0 across that 18x24 panel. Some board shops will do better than others, but in general impedance controlled microstrips are tougher to do well.

Ken Willis

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Author's Note: In modeling and simulating HSDD boards it is critical to get impedance, Z_0 , right. Yet here we have someone who is knowledgeable, telling us how difficult that is to do in reality. That says to me that we should provide very tolerant designs for products, and do something different for correlation studies to establish trust in an EDA tool. Correlation studies to establish trust in an EDA tool should be done off-line on boards especially designed to facilitate that activity.